In a capacitor and a capacitor array configured for reducing an effect of parasitic capacitance, the capacitor array can have a matrix configuration that includes a plurality of unit capacitors. The unit capacitors include a lower electrode and an upper electrode that constitute a plate capacitor, as well as shielding structures which enclose the capacitor. The unit capacitors are connected by an upper electrode connecting line with a first direction to constitute a plurality of capacitor columns, wherein the unit capacitors are also arranged in rows, in a second direction perpendicular to the first direction, and wherein lower electrode lead lines are disposed between the capacitor columns, the lower electrode lead lines being connected to the respective lower electrodes of each of the unit capacitors.

26 Claims, 12 Drawing Sheets