A Range-Scaled 13b 100MS/s 0.13um CMOS SHA-Free ADC Based on a Single Reference

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Abstract—This work describes a 13b 100MS/s 0.13um CMOS four-step pipeline ADC. The proposed SHA-free ADC employs a range-scaling technique based on switched-capacitor circuits properly to handle input signals twice as wide as a single on-chip reference range in the first pipeline stage. The range scaling makes reference driving buffers keep a sufficient dynamic voltage headroom and doubles the offset tolerance of a latched comparator without a pre-amp in the flash ADC1. The prototype ADC demonstrates the measured DNL and INL within 0.57LSB and 0.99LSB, respectively. The ADC shows a maximum SNDR of 64.6dB and a SFDR of 74.0dB at 100MS/s, respectively. The ADC with an active die area of 1.2mm² consumes 145.6mW including the high-speed reference buffers and 91mW excluding the buffers at 100MS/s and a 1.3V supply voltage.

Keywords— Analog-to-digital converter (ADC), pipeline, high resolution, SHA-free, range scaling, two-step reference selection.

I. INTRODUCTION

Recently a variety of wireless communication systems such as wireless local area network (IEEE 802.11b), wireless transmission, 3G and 4G wide-band code division multiple access (W-CDMA), and global system for mobile communication (GSM) have been developed corresponding to diverse user environment and needs. With the trend, high-performance analog-to-digital converters (ADCs) have been also highly demanded as an essential key building block in the system interface. Especially, the ADCs for 3G communication system applications require at least 12b resolution and a low power consumption.

Of various ADC architectures, the pipeline architecture has been commonly employed to meet the target specification of 12b and 100MS/s level [1]-[4]. Many inventive circuit techniques such as sample-and-hold amplifier (SHA)-free input network and signal range scaling have been developed to obtain high signal-to-noise ratio (SNR) and low power dissipation of the pipeline ADCs operating at a low supply voltage [5]-[10]. On the other hand, with the state-of-the art MOS processes still in progress, the decreased supply voltage tends to degrade the performance of analog circuits and particularly the available swing range of the input and output signals of an operational amplifier (op-amp) is considerably limited. From the thermal-noise point of view, the reduced input full-scale range in half requires four times as large as a sampling capacitance in the SHA for the same SNR performance, which increases the overall power consumption rapidly. Some range-scaling techniques can remove the power-hungry input SHA while handling a wide signal swing range even at a low supply voltage [8]-[10].

This work proposes a 13b 100MS/s CMOS pipeline ADC based on a range-scaling scheme for a 2VP-P input signal at a 1.3V supply voltage. The proposed range-scaling scheme needs only a single reference voltage as large as the internally processed signal range, which corresponds to a half of the full-scale input range. Thus, the buffers to drive the single reference voltage have a sufficient dynamic voltage headroom even at a low supply voltage simultaneously with low power and chip area. Since the range scaling based on switched-capacitor circuits doubles the offset tolerance of a comparator in the first-stage flash ADC, it is possible to use a latched comparator without a pre-amp. As a result, extra timing circuits are not required for high input sampling accuracy as frequently observed in the conventional SHA-free ADCs.

II. PROPOSED ADC ARCHITECTURE

The proposed 13b SHA-free four-step pipeline ADC is shown in Fig. 1. The range scaling technique is employed in the first pipeline stage to handle a wide input range of 2VP-P at a low supply voltage. The remaining pipeline stages are based on an attenuated signal swing of 1VP-P for stable operation with a high swing margin at a 1.3V supply voltage. The ADC employs only a pair of on-chip reference voltages, VREFT and VREFC, corresponding to 1VP-P. A simple latch-based comparator without a pre-amp properly decides 3b resolution in the flash ADC1 and the SHA-free input network does not suffer from the conventional sampling voltage mismatch. A gate-bootstrapping circuit for high linearity is also employed for sampling switches in both the MDAC1 and flash ADC1 [11]. In the back-end 5b flash ADC, two-step reference selection and interpolation schemes reduce both power and chip area furthermore [12].

![Fig. 1. Proposed 13b 100MS/s 0.13um CMOS ADC.](image)
III. CIRCUIT IMPLEMENTATION

A. MDAC1 for the Proposed Range-Scaling Technique

In the conventional pipeline ADCs using the same signal range for input and reference voltages, the 3b MDAC1 commonly amplifies a residue voltage by $2^2$ with four sampling capacitors and a feedback capacitor considering decision error correction from the flash ADC1. On the other hand, the 3b MDAC1 for the proposed range-scaling amplifies a residue voltage by 2 rather than $2^2$ with the same four sampling capacitors and a feedback capacitor, as shown in Fig. 2. During the sampling phase, an analog input is sampled on only two sampling capacitors, while remaining two sampling capacitors and a feedback capacitor are reset to a common-mode voltage ($V_{CM}$) as shown in Fig. 2(a). During the next amplifying phase, reference voltages are connected to all the sampling capacitors corresponding to the digital code from the flash ADC1 while the feedback capacitor is connected to the amplifier output as shown in Fig. 2(b). By sharing the sampled charge of four sampling capacitors, the signal gain of the MDAC1 is halved. At this time, the on-chip reference voltages, $V_{REFT}$ and $V_{REFC}$, are applied to the sampling capacitors to handle an input signal swing twice as wide as the internal reference range.

Each sampling capacitor in the MDAC1 is divided into two capacitor groups and each group consists of four smaller unit capacitors. Two groups of sampling capacitors for input and common-mode voltages are interdigitated for layout to average out a mismatch error between capacitors during the amplifying phase, as shown in the upper side of Fig. 2(a). Since the proposed 3b MDAC1 amplifies a residue voltage by 2 rather than $2^2$, an input signal of $2V_{P-P}$ is scaled down to $1V_{P-P}$ in the next pipeline stages. The remaining pipeline stages are implemented with the conventional topology.

B. Flash ADC1 with Improved Offset Tolerance

The 3b flash ADC1 in this work doubles the required 8 reference levels to handle input signals twice as wide as the on-chip reference, as shown in Fig. 3. Thus, the comparators for the proposed range-scaling scheme have twice the offset tolerance compared with those for the conventional scheme while a simple latched comparator without a pre-amp can be employed. The proposed 3b flash ADC1 consists of 16 synthesized reference generators, $X<0:15>$ and 8 latched comparators, $Y<0:7>$, as shown in Fig. 3. Each reference generator produces an output signal, $V_{OUTX}$, from two pairs of references and inputs. Two reference values are selected from $V_{REFT}$, $V_{REFC}$, and $V_{CMLR}$, while two input values are selected from $V_{INT}$, $V_{INC}$, and $V_{CM}$. The reference generator is actually implemented only with capacitors and MOS switches, as drawn in Fig. 4. The back-end latched comparators are properly processing an analog input of twice the on-chip reference range with 16 synthesized reference levels based on two pairs of input combinations.

![Fig. 3. Proposed 3b flash ADC1.](image)

![Fig. 4. Reference generator circuit.](image)
During the Q2 clock, two references of REF1 and REF2 are sampled on the sampling capacitors. During the next Q1 phase, two inputs of IN1 and IN2 are connected to the same capacitors. Then, the output voltage, $V_{OUTX}$, of the reference generator is derived as (1). The detailed input combinations for each reference generator are summarized in Table I.

$$V_{OUTX} = \frac{IN1 + IN2}{2} - \frac{REF1 + REF2}{2} + V_{CM} \tag{1}$$

**Table I. Four Input Combination for Each Reference Generator**

<table>
<thead>
<tr>
<th>REFERENCE GENERATOR</th>
<th>REF1</th>
<th>REF2</th>
<th>IN1</th>
<th>IN2</th>
<th>OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>x=0</td>
<td>V_CM</td>
<td>V_CM</td>
<td>V_CM</td>
<td>V_CM</td>
<td>V_CM</td>
</tr>
<tr>
<td>x=1</td>
<td>V_CM</td>
<td>V_CM</td>
<td>V_CM</td>
<td>V_CM</td>
<td>V_CM</td>
</tr>
<tr>
<td>x=2</td>
<td>V_CM</td>
<td>V_CM</td>
<td>V_CM</td>
<td>V_CM</td>
<td>V_CM</td>
</tr>
<tr>
<td>x=3</td>
<td>V_CM</td>
<td>V_CM</td>
<td>V_CM</td>
<td>V_CM</td>
<td>V_CM</td>
</tr>
</tbody>
</table>

Four outputs from the 16 synthesized reference output voltages in Fig. 3, $V_{OUTX}<0:15>$, are properly applied to the 8 back-end latched comparators, as shown in Fig. 5. Then, the differential output of a comparator, $(LP-LN)$, is derived as (2) and an analog input is compared with 8 reference levels within $\pm 2(V_{REFT}-V_{REFC})$ for 3b resolution. The final complementary comparator outputs, $T<0:7>$ and $C<0:7>$, are transferred to the MDAC1 through digital output buffers. The detailed inputs and outputs of each latched comparator are summarized in Table II. Moreover, two pull-down buffer switches between the input differential pair and regeneration nodes reduce the kick-back noise effect for improved comparison accuracy [13].

$$LP - LN = A0 \times \left( (LIN1 - LIN2) - (LIN3 - LIN4) \right) \tag{2}$$

(Where, $A0 =$ comparator gain)

**Table II. Inputs and Outputs of the Latched Comparator**

<table>
<thead>
<tr>
<th>LATCHED COMPARATOR</th>
<th>LIN1</th>
<th>LIN2</th>
<th>LIN3</th>
<th>LIN4</th>
<th>DIFFERENTIAL OUTPUT (LP-LN)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Y=0</td>
<td>V_CM</td>
<td>V_CM</td>
<td>V_CM</td>
<td>V_CM</td>
<td>A0 $\times \left( (V_{IN1} - V_{IN2}) - (V_{REF1} - V_{REF2}) \right)$</td>
</tr>
<tr>
<td>Y=1</td>
<td>V_CM</td>
<td>V_CM</td>
<td>V_CM</td>
<td>V_CM</td>
<td>A0 $\times \left( (V_{IN1} - V_{IN2}) - (V_{REF1} - V_{REF2}) \right)$</td>
</tr>
<tr>
<td>Y=2</td>
<td>V_CM</td>
<td>V_CM</td>
<td>V_CM</td>
<td>V_CM</td>
<td>A0 $\times \left( (V_{IN1} - V_{IN2}) - (V_{REF1} - V_{REF2}) \right)$</td>
</tr>
<tr>
<td>Y=3</td>
<td>V_CM</td>
<td>V_CM</td>
<td>V_CM</td>
<td>V_CM</td>
<td>A0 $\times \left( (V_{IN1} - V_{IN2}) - (V_{REF1} - V_{REF2}) \right)$</td>
</tr>
</tbody>
</table>

C. Comparison of Various Range-Scaling Techniques

The proposed and some previously reported range-scaling techniques are compared in Table III. The proposed range-scaling technique doubles the number of capacitors in the flash ADC1, while a resistor string consuming a DC current in the flash ADC1 is not needed. The reference buffers have a sufficient voltage headroom where the proposed scheme employs only a single on-chip reference voltage corresponding to a half of the input signal range. The comparators of the flash ADC1 in the first pipeline stage compare an input signal with the increased reference levels by twice based on switched-capacitor circuits. Due to the doubled offset tolerance in the comparator, a latched comparator without a pre-amp can be used in the flash ADC1 without additional timing circuits for high input sampling accuracy.

**Table III. Comparison of Various Range-Scaling Schemes**

<table>
<thead>
<tr>
<th>MDAC1</th>
<th># of Capacitors</th>
<th>Feedback Factor</th>
<th>Comparator Offset Tolerance</th>
<th>Voltage Headroom of REF Buffers</th>
</tr>
</thead>
<tbody>
<tr>
<td>FLASH ADC1</td>
<td>8</td>
<td>N</td>
<td>2N</td>
<td>Insufficient</td>
</tr>
<tr>
<td>Comparator Offset Tolerance</td>
<td>2A</td>
<td>A</td>
<td>2A</td>
<td></td>
</tr>
<tr>
<td>Voltage Reference</td>
<td>0</td>
<td>X</td>
<td>X</td>
<td>Insufficient</td>
</tr>
</tbody>
</table>

D. Measured Results

The prototype 13b 100MS/s ADC is implemented in a 0.13um CMOS technology as shown in Fig. 6. The ADC with an active die area of 1.2mm$^2$ dissipates 145.6mW including on-chip reference buffers and 91mW excluding buffers at 100MS/s and a 1.3V supply voltage. The measured differential nonlinearity (DNL) and integral nonlinearity (INL) are within $\pm 0.57$LSB and $\pm 0.99$LSB, respectively, as shown in Fig. 7. As plotted in Fig. 8, the measured signal-to-noise-and-distortion ratio (SNDR) and spurious-free dynamic range (SFDR) at 100MS/s with a 4MHz input sine wave are 64.6dB and 74.0dB, respectively. The SNDR and SFDR are maintained over 50.4dB and 64.0dB, respectively, at the Nyquist input frequency. The figure of merits, defined as $Power/(2^{ENOB} \times fs)$, of the prototype ADC is 0.66pJ/conversion-step excluding on-chip reference buffers. The overall ADC performance is summarized in Table IV.

**Table IV. Measured Results**

TBD
V. CONCLUSION

This work proposes a 13b 100MS/s 0.13um CMOS SHA-free four-step pipeline ADC. The proposed range-scaling scheme using switched-capacitor circuits properly handles an input signal range twice as wide as an on-chip signal swing based on a single reference voltage. The prototype ADC shows a maximum DNL and INL within 0.57LSB and 0.99LSB, respectively. The ADC shows a maximum SNDR of 64.6dB and a maximum SFDR of 74.0dB at 100MS/s, respectively.

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