A 12b 60MS/s 0.11μm Flash-SAR ADC Using a Mismatch-Free Shared Sampling Network

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Abstract—This work proposes a 12b 60MS/s 0.11μm CMOS Flash-SAR ADC for wireless communication systems. The proposed Flash-SAR ADC is implemented with a 4b flash ADC and a 9b SAR ADC for high speed operation with low power consumption. Furthermore, the shared single sampling-network minimizes a sampling-time mismatch between the flash ADC and the SAR ADC, which is commonly observed in a Flash-SAR ADC without a T/H circuit. The prototype ADC occupies an active die area of 0.31mm² and consumes 3.2mW at a 1.2V supply voltage.

Keywords—analog-to-digital converter (ADC); shared single network; sampling-time mismatch

I. INTRODUCTION

Recently, the demand for high-performance analog-to-digital converters (ADCs) has greatly increased for wireless communication system applications such as WiMAX and WiFi. The ADCs for such applications require at least 12b resolution and a conversion rate exceeding 50MS/s with a small chip area and a low power dissipation. The successive-approximation register (SAR) ADCs mostly based on digital circuits has been widely used due to high power efficiency and small chip area with scaling-down CMOS technologies. On the other hand, the conversion rate of the SAR ADC is somewhat limited by iterative operations. To enhance the conversion rate, the hybrid architectures such as pipelined-SAR and Flash-SAR ADCs are commonly used. Among these architectures, the Flash-SAR ADC tends to be more competitive than the pipelined-SAR ADC as for power consumption.

II. PROPOSED ADC ARCHITECTURE

The proposed 12b 60MS/s Flash-SAR ADC consists of a C-R hybrid digital-to-analog converter (DAC), a comparator, a 4b flash ADC, digital control logic circuits, on-chip current and voltage references (I/V) references, and a digital correction logic (DCL) block, as shown in Fig. 1. The proposed ADC reduces an internal operation speed by using the flash ADC for the 4 most significant bits (MSBs) during one clock period. The shared single sampling-network is employed to minimize a sampling-time mismatch between the flash ADC and the SAR ADC. The C-R hybrid DAC of the SAR ADC employs a simple resistor string [1], a 2-step split-capacitor array, and a common-mode voltage (Vcm)-based switching scheme [2] to minimize chip area and power consumption. An interpolation technique implemented in the 4b flash ADC halves the required number of pre-amplifiers, reducing chip area and power consumption. Moreover, the switched-bias power-reduction technique turns off the idle comparators of the flash ADC during SAR operation.

III. CIRCUIT IMPLEMENTATION

A. Proposed Mismatch-Free shared sampling-network.

The performance of a conventional Flash-SAR ADC without a track-and-hold (T/H) circuit can be degraded by a sampling-time mismatch between the flash ADC and the SAR ADC [3]. The proposed ADC replaces the function of a T/H with a single sampling network which is shared between the flash ADC and the SAR ADC, as shown in Fig. 2. Therefore, a sampling-time mismatch between the flash ADC and the SAR ADC is fundamentally removed, while power consumption and chip area are minimized.
number of unit capacitors in the capacitor array. Furthermore, the number of unit capacitors is reduced by a $V_{CM}$-based switching scheme and a simple resistor string to decide the last two LSBs in the C-R hybrid DAC. Meanwhile, a high operation speed of the SAR ADC is restricted due to the DAC settling time caused by the MSB capacitor size [4]. The MSB capacitor size is determined by a resolution of the SAR ADC. In this work, a thermometer capacitor array composed of fourteen of $4C_U$ is employed for three MSB capacitors of $32C_U$, $16C_U$, and $8C_U$ to reduce the DAC settling time. As a result, the DAC settling time is determined by $4C_U$ rather than the MSB capacitor $32C_U$.

B. Operation timing of the proposed ADC

The timing diagrams of the conventional 12b 60MS/s SAR ADC and the proposed 12b 60MS/s Flash-SAR ADC are compared in Fig. 3. In the conventional SAR ADC, the internal clock operates 13 times as fast as the conversion rate of the overall ADC. Therefore, the conversion rate is limited by the proportionally increased internal operation speed. However, in the proposed SAR ADC, a 4b flash ADC decides the 4 MSBs during one clock period simultaneously with an input sampling to reduce the internal operation speed of the conventional SAR ADC. As a result, the internal operation speed of the proposed Flash-SAR ADC is reduced by 15%, compared with that of the conventional SAR ADC.

IV. SIMULATION RESULTS

The proposed 12b 60MS/s Flash-SAR ADC is implemented in a 0.11μm CMOS process as shown Fig. 4. The simulated ADC with an active die area of 0.31mm$^2$ consumes 3.2mW excluding on-chip I/V references. When multi-purpose on-chip I/V references for various applications are included, the ADC has an active die area of 0.45mm$^2$ and a power consumption of 6.9mW. The simulation results of the proposed Flash-SAR ADC in a 0.11μm CMOS are summarized in Fig. 5. When 5 major input signals, $V_{IN}$, are sampled at a sampling frequency of 60MS/s, $C_{SAM}$, each input signal is accurately converted into a corresponding digital output of 12b as expected with an input range of $1.4V_{PP}$ at a 1.2V supply voltage.

V. CONCLUSIONS

This work proposes a 12b 60MS/s 0.11μm CMOS Flash-SAR ADC for wireless communication systems. The proposed Flash-SAR ADC combines a high speed of the 4b flash ADC with a low power of the 9b SAR ADC. The 4b flash ADC reduces the internal operation speed of the SAR ADC since the 4MSBs are simultaneously decided. The shared input sampling-network minimizes a sampling-time mismatch between the flash ADC and the SAR ADC. The simulated ADC occupies an active die area of 0.31mm$^2$ and consumes 3.2mW at a 1.2V supply voltage.

REFERENCES


