A 12b 50MS/s 10.2mA 0.18μm CMOS Nyquist ADC with a Fully Differential Class-AB Switched OP-AMP

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Abstract

A 12b 50MS/s pipelined ADC based on a fully differential class-AB switched op-amp achieves low power consumption with a high differential input range of 2.4Vp-p. The proposed input sampling network samples wideband signals exceeding the Nyquist frequency without a SHA. The prototype ADC in a 0.18μm CMOS shows a power dissipation of 18.4mW at 50MS/s and 1.8V with an active die area of 0.26mm². Keywords: ADC, Nyquist, Differential, and Class-AB

Introduction

Recently, low power consumption has become one of the most significant requirements for battery-powered mobile applications. On the other hand, broadcasting systems such as DVB-H, DVB-T, SDMB, and TDMB require an input bandwidth exceeding the Nyquist frequency with a signal dynamic range higher than 1.5Vp-p [1]. In such portable applications, one of the most critical blocks simultaneously to obtain low power consumption, wide input bandwidth, and high dynamic range is op-amp. Op-amp needs a proper slewing and settling time for signals to reach a target level. Conventional class-A op-amps continuously consume static currents during the entire operating interval, while class-AB type op-amps consume mostly dynamic currents during the short slewing period for output signals to reach nearly a target voltage. During the signal settling time after slewing, op-amps consume only small quiescent currents. In addition, class-AB op-amps tend to have a lot of merits from the standpoint of transistor size and die area with reference to the same operating speed [2].

This work proposes a low-power ADC based on a fully differential class-AB switched op-amp with floating current-source biasing and attenuated dynamic-common-mode feedback (CMFB) circuits. The proposed op-amp can process signals with a higher dynamic range than conventional fully differential CMOS op-amps of folded-cascode or telescopic types.

Proposed ADC Architecture and Implementation

The proposed 12b 50MS/s 1.8V ADC, based on a 2.5-bit/stage pipelined architecture, consists of five multiplying D/A converters (MDACs), six flash ADCs, a bias generator, and a current reference for stand-alone operation without any other external circuits, as shown in Fig. 1. The proposed ADC employs a SHA-free structure using the identical bootstrapping clock phases for both of the MDAC1 and FLASH1 inputs, as shown in the bottom of Fig. 1. The proposed SHA-free structure can sample input frequencies higher than the Nyquist frequency even without a separate SHA by using the same timing clock in the MDAC1 opamp and the FLASH1 comparator.

The proposed fully differential class-AB op-amp with a switched op-amp technique is employed in all the MDAC blocks of Fig. 1. As shown in Fig. 2, the proposed op-amp has four functional sections of a complementary input block, cascaded gain stages, output swing blocks, and CMFB circuits. The floating current nodes of T3, T4, T5, and T6, are automatically settled by the CMFB system with a differential class-AB control circuit. This op-amp employs cascoded-Miller compensation technique. During the sampling phase, four MOSFET switches, M7 to M10, connected to OUT+ and OUT-, are off. At the same time, both differential output nodes, OUT+ and OUT-, are set to VCOM as shown in Fig. 1. The gates of M11 and M13 are connected to T1 while the gates of M12 and M14 are connected to T2, to achieve a fast op-amp signal settling behavior in the next clock phase. As results, the proposed switched op-amp technique minimizes the static currents required in the output stage and reduces the power dissipation of the entire op-amp without degrading the signal settling time. The gain stage is basically composed of a floating control scheme and a cascoded-Miller compensation circuit [2].

Since a fully dynamic CMFB circuit can generate stability problems due to the CMFB gain to outputs with transistors M15 and M16, the proposed op-amp implements attenuated dynamic CMFB circuits to reduce the CMFB gain. The CMFB1 and CMFB2 signals in Fig. 2 are generated in the top and bottom CMFB blocks, respectively. Each CMFB signals are connected to VB1 and VB4 during the sampling phase for op-amp reset. The op-amp employs non-overlapped clocks, Q1 and Q2, for sampling and amplifying operation.

Measured Performance of The Prototype ADC

The prototype ADC is designed and implemented in a 0.18μm single-poly six-metal CMOS process. It consumes 10.2mA at 50MS/s with a 1.8V power supply. The active die area is 0.26mm² (=700μm × 370μm), as shown in Fig. 3. As illustrated in Fig. 4, the measured DNL and INL are within ±0.26 LSB and ±0.72 LSB, respectively. At a sampling frequency of 50MHz, the measured SNDR and SFDR are 64.0dB and 76.6dB, respectively, with 2.4Vp-p and a 31MHz input signal, as plotted in Fig. 5.

The proposed differential class-AB opamp based ADC shows no abrupt performance degradation even though the sampling frequency is increased to 100MHz, twice the current target sampling frequency of 50MHz, as shown in Fig. 6. The overall ADC performance is summarized in Table I.
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References


Fig. 1. Proposed ADC and input sampling network.

Fig. 2. Proposed fully differential class-AB switched op-amp.

Fig. 3. Die photo of the proposed ADC.

Fig. 4. Measured DNL and INL.

Fig. 5. Measured FFT plot (fIN = 31MHz and fS = 50MHz).

Fig. 6. Measured SFDR and SNDR (fIN = 4MHz).

Table I. Performance summary of the proposed ADC