A 52mW 0.56mm² 1.2V 12b 120MS/s SHA-Free Dual-Channel Nyquist ADC Based on Mid-Code Calibration

Hee-Cheol Choi¹, Young-Ju Kim¹, Se-Won Lee¹, Jae-Yeol Han¹, Oh-Bong Kwon², Younglok Kim¹, and Seung-Hoon Lee¹
¹Dept. of Electronic Engineering, Sogang University, Seoul, Korea
²MagnaChip Semiconductor, Seoul, Korea

Abstract—This work describes a 12b 120MS/s dual-channel SHA-free Nyquist ADC based on a mid-code calibration technique eliminating offset mismatch between channels. The prototype ADC achieves a peak SNDR of 61.1dB and a peak SFDR of 74.7dB for input frequencies up to 60MHz at 120MS/s. Also, the measured DNL and INL are within ±0.30LSB and ±0.95LSB, respectively. The ADC fabricated in a 0.13μm CMOS process occupies an active die area of 0.56mm² and consumes 51.6mW.

I. INTRODUCTION

High-resolution and high-speed ADCs have been increasingly in demand for various communication, CIS, and display applications. Some state-of-the-art digital TVs require the ADCs with a resolution of up to 12b and a sampling rate exceeding 110MS/s. Specifically, low-power and small-size requirements together with a high sampling rate have been the key design issues for high-quality video signal processing systems employing several ADC units on the same die. Recently reported single-channel pipeline ADCs can achieve a 12b resolution at a 100MS/s level, but they tend to need relatively high power and large chip area [1]-[4]. On the other hand, the time-interleaved ADC architecture is an effective way to implement a high sampling rate ADC with low power, but offset, gain, and sampling time mismatches between channels have typically limited ADC performance. Although inventive calibration techniques can minimize the offset and gain mismatch of a multi-channel ADC, circuit complexity for calibration increases proportionally to the number of channels and mismatch sources [5]. The proposed ADC and the recently reported 12b CMOS ADCs with a sampling rate exceeding 50MS/s are plotted in Fig. 1.

Fig. 1. Performance comparison of recently reported 12b ADCs.

II. PROPOSED ADC ARCHITECTURE

The proposed 12b 120MS/s dual-channel ADC without a front-end SHA meets the needs of both low power consumption and small chip size. The ADC has two channels of a single ADC operating at a sampling rate of 60MS/s with an externally controlled 2-phase 60MHz input clock to remove the sampling timing mismatch error. The offset mismatch between two ADC channels is eliminated by a digital mid-code calibration based on a simple digital circuit with short calibration time. The gain mismatch between channels is minimized with a SHA-free architecture and a matched and symmetrical layout. In particular the proposed parallel architecture without an input SHA, can be effectively applied to time-interleaved ADC and multi-channel AFE, where ADCs need to process signals simultaneously at a high speed, in such applications as mega-pixel CIS [6].

As shown in Fig. 2, the proposed dual-channel ADC consists of two 12b 60MS/s single-channel ADCs with off-chip mid-code calibration logic (MC CAL) and two clock phases of CLK and CLKB. Calibration starts when the positive and negative inputs of each channel are tied together with "CAL" high. The offset error of each ADC channel is measured separately by averaging digital outputs by 16 times after the pipeline delay of four clock cycles. Each averaged digital code is subtracted from the ideal 2048 code and the results (DAOFFSET, DBOFFSET) are stored in memory.

Fig. 2. Block diagram of proposed dual-channel ADC.
Fig. 3. Functional description of mid-code digital calibration.

During normal conversion, each measured and stored offset is subtracted from raw digital outputs of each ADC channel and the calibrated digital output from each channel is time-interleaved by a digital MUX block. The digital mid-code calibration concept is briefly described in Fig. 3. Before calibration, additional noise tones appear at $[fs/2]$ due to channel-offset mismatch and at $[fs/2-fin]$ due to gain and sampling time mismatches, respectively. Normalized minimum magnitude of each noise tone can be summarized as (1) and (2).

$$T_{OFFSET} = 20 \log \left( \frac{|DAOFFSET - DBOFFSET|}{2^N} \right)$$  (1)

$$T_{GAIN} = 20 \log \left( \frac{|GAERROR - GBERROR|}{2^N} \right)$$  (2)

The external clock is carefully controlled to eliminate the noise tone from sampling time mismatch. The spurious tone due to gain error ($T_{GAIN}$) comes from the difference of average gain in two ADC channels [7]. The proposed ADC architecture without SHA and resistor ladder can remove the gain error without any calibration scheme.

III. ADC CIRCUIT IMPLEMENTATION

The power- and area-optimized single-channel 12b 60MS/s pipeline ADC without a SHA is shown at the bottom of Fig. 2. The ADC consists of five multiplying DACs (MDACs), six FLASH ADCs, on-chip current reference, and other supplementary circuits. In conventional multi-channel pipeline ADCs, the primary gain mismatch comes from the SHA gain error and the different top and bottom reference voltages supplied to each functional circuit block. The capacitor mismatch of SHA also contributes to the gain error. This work proposes a SHA-free input sampling network and a resistor-free FLASH ADC architecture to remove the gain mismatch caused by the SHA and the current in the resistor ladder of FLASH ADCs. Although input frequencies of the conventional SHA-free ADCs can be restricted to several MHz due to the sampling-time error of the MDAC1 and FLASH ADC1, the prototype ADC also eliminates this problem with the proposed input sampling network as shown in Fig 4.

Fig. 4. Simplified input sampling network of MDAC1 and FLASH ADC1.

The sampling-time mismatch error is removed by synchronizing the sampling time of the switches connected to the bottom plate of each capacitor in the MDAC1 and the FLASH ADC1 with a bootstrapping clock (Q1BS). The MDAC1 has open loop sampling architecture with a two-stage op amp to achieve a 12b level accuracy at wideband inputs. The second stage op amp employs switched op amp architecture to minimize power consumption [8]. The proposed capacitor-divider (C-DIV) based comparator is illustrated at the bottom of Fig. 4. With this comparator, the FLASH ADCs can be implemented without a resistor divider. The unit capacitors are connected only to the top and bottom reference voltages, REF+ and REF-, selectively. The coding of the proposed ADC is described in Fig. 5. The FLASH
ADC of stage 1 employs three comparators, while the remaining stages employ five comparators. All the FLASH ADCs consist of the same C-DIV type comparators and the bootstrapping clock is applied only to the first FLASH ADC. The schematic of resistor-free FLASH ADC2 to ADC6 is illustrated at the bottom of Fig. 5.

IV. PROTOTYPE ADC MEASUREMENTS

The prototype ADC is fabricated by a 0.13µm CMOS process. Both of the channels are symmetrically laid out as illustrated in Fig. 6. The reduced number of dummy capacitors and the resistor-free FLASH ADCs contribute to the reduced area of passive components occupying relatively large portion of the whole chip area. The active die area of the dual-channel ADC excluding off-chip calibration logic is 0.56mm².

Fig. 7 and Fig. 8 illustrate the measured static linearity performance of the two separate ADC channels and the dual-channel time-interleaved ADC. The proposed dual-channel ADC shows better linearity than each single-channel ADC, since the random linearity errors of each single-channel ADC are also averaged out. The proposed offset calibration does not affect the linearity of the proposed ADC, as illustrated in Fig. 8.

![Fig. 5. Coding technique of proposed FLASH ADC.](image)

![Fig. 6. Die micrograph of dual-channel ADC.](image)

![Fig. 7. Measured DNL and INL of each ADC channel.](image)

![Fig. 8. Measured DNL and INL of proposed dual-channel ADC.](image)

The FFT spectrums of two single-channel ADCs and the dual-channel ADC are plotted in Fig. 9. The input signal frequency is 59.9MHz, while the sampling rate of each single channel is 60MS/s to achieve a 120MS/s sampling rate in the overall ADC. The spurious components in the dotted circle at [fs/2-fin] in the left of the bottom graphs in Fig. 9 are caused...
by gain mismatch between channels in time-interleaved ADC. The value of 88.0dBc indicating gain mismatch is negligibly small and independent of calibration. On the other hand, the harmonic component of [fs/2] indicating offset mismatch is 49.9dBc before calibration, which limits the SFDR. The measured channel offset of the prototype ADC corresponds to 13 LSBs at 12b. The offset spurious tone is improved to 82.7dBc after the proposed mid-code calibration.

The SNDR and SFDR versus sampling frequencies for a 5MHz input are plotted in Fig. 10. The SNDR and SFDR maintain better than 60dB and 70dB up to 120MS/s, respectively.

The prototype dual-channel ADC consumes 51.6mW at 120MS/s and 1.2V. The measured DNL and INL of the calibrated dual-channel ADC are within ±0.30LSB and ±0.95LSB, respectively. The measured SNDR and SFDR are 63.6dB and 81.0dB, respectively, with an input frequency of 5MHz and a sampling rate of 20MS/s. At a sampling rate of 120MS/s, the measured SNDR and SFDR are 61.1dB and 74.7dB for a 59.9MHz input frequency, respectively. The FOM defined as Power/(2 ENOB˜fS), is 0.46pJ/conversion-step. The proposed ADC performance is summarized in Table I.

V. CONCLUSION

This work proposes a 12b 120MS/s dual-channel ADC based on a mid-code calibration technique eliminating offset mismatch between channels. The ADC also employs SHA- and resistor-free architecture for reduced gain mismatch between channels and small die area. The proposed 12b Nyquist-rate ADC shows a 120MHz sampling rate with 51.6mW power consumption and 0.56mm² active die area.

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REFERENCES