Calibrated 10 b 28 nm CMOS SAR ADC based on integer-based split capacitors

E.-C. Lee, T.-J. An, J.-S. Park, G.-C. Ahn and S.-H. Lee

A calibrated 10 b 5 MS/s 28 nm CMOS successive-approximations-register ADC based on an integer-based split capacitor array is presented. The proposed ADC employs a split capacitor array to optimise the overall power consumption, chip area and linearity performance. An attenuation capacitor between two capacitor arrays is implemented with an integer multiple of unit capacitors rather than a fraction of unit capacitors. The proposed calibration of capacitors reduces the non-linearity error caused by device mismatches in the conventional split capacitor array. The measured prototype ADC which has an active die area of 0.063 mm² shows a maximum signal-to-noise-and-distortion ratio and spurious-free dynamic range of 59.25 and 70.44 dB, respectively, and consumes 42.5 μW at 0.7 V and 5 MS/s. Moreover, the measured differential non-linearity (NL) and integral non-linearity (INL) are within 0.36 and 0.52 least significant bit, respectively, after calibration.

Introduction: Recently, there has been a growing interest in the Internet of things (IoT), which links to the inter-object network to provide faster and more immediate service. To optimise IoT applications, it is necessary to further develop small, low-power ADCs with a resolution of 10 b or higher and an operation speed of several MS/s. To meet these requirements, successive-approximations-register (SAR) ADCs are frequently used as they are more competitive in terms of power consumption and chip area than a pipeline, delta-sigma or algorithmic-structure ADCs thanks to the nanometre-scaled CMOS process. In this Letter, to address growing needs in IoT applications, a 10 b 5 MS/s SAR ADC with a low voltage of 0.7 V is presented. The proposed ADC reduces the number of unit capacitors (\(C_u\)) as well as the chip area and power consumption by utilising DACs with an integer-based split capacitor array. In addition, the proposed ADC realises attenuation capacitors (\(C_x\)) as an integer multiple of \(C_u\), which is in contrast to \(C_u\) of the conventional split capacitor array. At the same time, the proposed ADC employs calibration using variable capacitors (\(C_v\)) in order to minimise non-linearity (NL) caused by the parasitic capacitance at the top plate of the least significant bit (LSB) capacitor array.

Proposed ADC structure: The proposed ADC is composed of the capacitor arrays, calibration DACs, a comparator and an SAR logic as shown in Fig. 1. The capacitor array of the proposed ADC is based on an integer-based split capacitor array. The most SB (MSB) array and the LSB array determine 6 and 4 b, respectively. By applying \(C_u\), which is an integer multiple of \(C_x\), the proposed ADC is able to minimise linearity degradation caused by mismatches between \(C_x\) and the capacitor array, as often observed in conventional split capacitor arrays. Commonly, a split capacitor array using \(C_u\) degrades linearity performance due to the parasitic capacitance at the top plate of LSB array and \(C_u\). However, the capacitor array of the proposed ADC alleviates this issue by instead applying \(C_x\) for calibration on the LSB array. Furthermore, by applying the composite switching method \([2]\) and simultaneously using the least capacitor of the LSB capacitor array with two capacitors serially, the proposed ADC is able to reduce the required MSB capacitor as \(2C_u\). As a result, the total number of capacitors employed in the capacitor array of the proposed ADC is 77, which is just 7.5% of 1024 required for the conventional 10 b binary-weighted capacitor array.

Split capacitor array with an integer multiple of \(C_u\) and calibration: The conventional split capacitor array often degrades linearity due to the capacitor mismatch between the capacitor array and \(C_u\), which is a non-integer multiple of \(C_u\), as shown in Fig. 2a. There are existing techniques \([3]\) to alleviate linearity degradation by integrating \(C_u\) as to be an integer multiple of \(C_u\). However, there is still a limit to the number of \(C_u\) that can be reduced. The proposed capacitor array reduces the number of \(C_u\) to 77 by setting \(C_u\) as an integer multiple of \(C_u\). In this case, the dummy capacitors of 4\(C_u\), which are additionally required for the LSB array for the binary-weighted capacitor array, are employed as \(C_x\) for calibration.

Fig. 1 Proposed 10 b 5 MS/s 28 nm CMOS SAR ADC

Fig. 2 Proposed split capacitor array with integer multiple of \(C_u\)

a Conventional split capacitor array

b Split capacitor array with 4-unit attenuation capacitors

However, the proposed ADC can have a different weighted value for the LSB array (\(W_{lsb}\)) due to the parasitic capacitance at the top plate of the LSB array (\(C_{pl}\)) and the parasitic capacitance of the \(C_u\) (\(C_{pu}\)) as shown in (1), (2) and Fig. 3. The error of the weighted value for the LSB array (\(W_{lsb, error}\)) is calculated in (2), and the greater the difference between \(W_{lsb}\) and \(W_{lsb, error}\), the worst the linearity of the proposed ADC

\[
W_{lsb} = \frac{C_A}{C_{lsb} + C_A + C_X} \tag{1}
\]

\[
W_{lsb, error} = \frac{C_A + C_{pu}}{C_{lsb} + C_A + C_X + C_{pl}} \tag{2}
\]

Fig. 3 Parasitic capacitance of proposed split capacitor array

Therefore, the proposed ADC employs a calibration scheme using the variable capacitor topology as shown in Fig. 4 to alleviate the linearity degradation caused by \(C_{pl}\) and \(C_{pu}\). The variable capacitor topology for \(C_X\) is composed of 17 unit capacitors of \(C_u\) aligned in a binary-weighted structure as shown in Fig. 4b, and the capacitance of \(C_x\) is controlled by a 5 b external digital code. Accordingly, if \(W_{lsb, error}\) occurs due to \(C_{pl}\) and \(C_{pu}\), as shown in Fig. 4a, the calibration is performed to ensure the values of \(W_{lsb}\) and \(W_{lsb, error}\) have the approximately same values by adjusting the capacitance of \(C_X\).

Fig. 4 Proposed variable capacitor

a Calibration procedure

b Topology

Measured results: The proposed calibrated 10 b 5 MS/s SAR ADC is implemented in a 28 nm CMOS process. The prototype ADC...
occupies an active die area of 0.063 mm² and the layout is shown in Fig. 5.

<table>
<thead>
<tr>
<th>Technology (nm)</th>
<th>Resolution (b)</th>
<th>Speed (MS/s)</th>
<th>Supply (V)</th>
<th>Power (μW)</th>
<th>Effective number of bits (bits)</th>
<th>DNL (LSB)</th>
<th>INL (LSB)</th>
<th>Area (mm²)</th>
<th>Figure of merit (D/Con.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>180</td>
<td>10</td>
<td>0.768</td>
<td>1.8</td>
<td>58</td>
<td>9.83</td>
<td>0.55</td>
<td>0.77</td>
<td>0.010</td>
<td>74</td>
</tr>
<tr>
<td>130</td>
<td>10</td>
<td>1</td>
<td>0.8</td>
<td>9</td>
<td>8.8</td>
<td>0.56</td>
<td>0.61</td>
<td>0.056</td>
<td>20</td>
</tr>
<tr>
<td>150</td>
<td>10</td>
<td>1</td>
<td>0.9</td>
<td>22.1</td>
<td>9.07</td>
<td>0.56</td>
<td>0.69</td>
<td>0.056</td>
<td>20.6</td>
</tr>
<tr>
<td>180</td>
<td>10</td>
<td>2</td>
<td>0.7</td>
<td>9.3</td>
<td>8.81</td>
<td>0.47</td>
<td>0.61</td>
<td>0.056</td>
<td>20.6</td>
</tr>
<tr>
<td>90</td>
<td>10</td>
<td>4</td>
<td>0.7</td>
<td>42.5</td>
<td>8.11</td>
<td>0.36</td>
<td>0.61</td>
<td>0.056</td>
<td>20.6</td>
</tr>
<tr>
<td>28</td>
<td>10</td>
<td>5</td>
<td>0.7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0.056</td>
<td>20.6</td>
</tr>
</tbody>
</table>

The measured static and dynamic performances of the prototype ADC are shown in Figs. 6 and 7. The differential NL (DNL) and integral NL (INL) in Fig. 6a have large transitions in every 32-code cycles due to $C_{PL}$ and $C_{PA}$. However, in the DNL and INL after calibration as shown in Fig. 6b, the transitions which used to occur in every 32-code cycles do not exist. In addition, harmonics generated in the fast Fourier transform (FFT) waveform in Fig. 7a are removed after calibration as seen in the FFT waveform in Fig. 7b. As a result, the measured maximum DNL and INL are enhanced from 0.88 to 0.36 and 1.72 to 0.52 LSB, respectively. The measured signal-to-noise-and-distortion ratio (SNDR) and spurious-free dynamic range (SFDR) are also improved from 48.17 to 59.25 and 60.15 to 70.44 dB at the Nyquist frequency, respectively. The performance summary and comparison of the prototype ADC are summarised in Table 1.

| Conclusion: | This Letter proposes a low-power, small-area and high-linearity calibrated 10 b 5 MS/s SAR ADC for IoT applications implemented in a 28 nm CMOS process. The proposed ADC adopts a DAC structure with an integer-based split capacitor array to realise a low-power and small-area ADC. Furthermore, by employing a calibration scheme based on the variable capacitor to the LSB array, the proposed ADC is able to reduce linearity degradation caused by the parasitic capacitance of the top plate of the LSB array and $C_A$, thereby achieving high linearity. The proposed ADC is implemented in a 28 nm CMOS process, and the active die area of the chip is 0.063 mm². The measured DNL and INL are 0.36 and 0.52 LSB, respectively, and the maximum dynamic performance at the sampling rate of 5 MS/s is 59.25 dB SNDR and 70.44 dB SFDR. The proposed ADC consumes 42.5 μW at the power voltage of 0.7 V.

| Acknowledgments: | This work was supported by the Samsung Electronics, the IDEC of KAIST, the Ministry of Trade, Industry & Energy (Project no. 10080488) and the Korea Semiconductor Research Consortium support program for the development of the future semiconductor device.

References