A 14b 150 MS/s 140 mW 2.0 mm² 0.13 µm CMOS A/D converter for software-defined radio systems

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ABSTRACT

This work proposes a 14 b 150 MS/s CMOS A/D converters (ADC) for software-defined radio systems requiring simultaneously high-resolution, low-power, and small chip area at high speed. The proposed calibration-free ADC employs a wide-band low-noise input sample-and-hold amplifier (SHA) along with a four-stage pipelined architecture optimizing scaling-down factors for the sampling capacitance and the input trans-conductance of amplifiers in each stage to minimize thermal noise effect and power consumption. A signal-insensitive 3-D fully symmetric layout achieves a 14 b level resolution by reducing a capacitor mismatch of three MDACs. The prototype ADC in a 0.13 µm 1P8M CMOS technology demonstrates a measured differential nonlinearity (DNL) and integral nonlinearity within 0.81LSB and 2.83LSB at 14 b, respectively. The ADC shows a maximum signal-to-noise-and-distortion ratio of 64 and 61 dB and a maximum spurious-free dynamic range of 71 and 70 dB at 120 and 150 MS/s, respectively. The ADC with an active die area of 2.0 mm² consumes 140 mW at 150 MS/s and 1.2 V. Copyright © 2010 John Wiley & Sons, Ltd.

1. INTRODUCTION

Recently many different circumstances and various needs of users in the digital world have accelerated the advent of numerous wireless communication system standards with greatly efficient and flexible transceiver technologies. Especially, the software-defined radio (SDR) system has been developed as one of the most powerful next-generation wireless communication technologies, unifying diverse communication system standards based on software programming of high-performance digital signal processing units without modifying specific hardware. The SDR technologies replace conventional analog-based signal processing such as down conversion and channel filtering with digital-based signal processing. It allows the overall system to reduce the number of analog functional blocks with high power consumption and large chip area and simultaneously to enhance system efficiency and integrating capability. For those SDR applications, high-performance A/D converters (ADCs) with high enough resolution and wide enough bandwidth are essential to convert analog signals with intermediate frequency bandwidth into digital bits, at the forefront-end location of the overall system if possible. Although the specifications can be considerably variable depending on the employed SDR systems, the ADCs commonly need at least 14 b-level resolution and a sampling rate exceeding 100 MS/s along with small chip area and low-power dissipation to be integrated with large-scaled digital circuits such as programmable down conversion units and SDR processors.

Of various well-known ADC architectures, the pipelined ADC architecture is one of the best candidates to achieve the target resolution and sampling rate. However, a maximum achievable accuracy has been limited in conventional CMOS pipelined ADCs and a variety of analog- and digital-domain calibration techniques and hybrid processes such as Bi-CMOS have been widely adopted to realize a high resolution of 14 b level. Additional electronic

calibration techniques with complicated algorithm and hardware tend to increase circuit complexity and chip area, while huge power consumption is unavoidable when employing Bi-CMOS processes. Recently reported ADCs exceeding a 40 MS/s conversion rate at a 14–15 b resolution are compared with the proposed ADC in Table I [1–10]. As shown in Table I, the ADC using an analog domain calibration technique [1] occupies a chip area of 16 mm^2 while another ADC implemented with a Bi-CMOS technology [8] consumes 1.85 W at 125 MS/s. The proposed ADC quite suitable for SDR system integration illustrates the lowest power consumption of 140 mW at the lowest supply voltage of 1.2 V among the 14 b ADCs reported up to now while occupying a chip area of 2.0 mm^2.

In this work, a low-noise high-gain input sample-and-hold amplifier (SHA) with flip-around two capacitors is followed by a calibration-free four-stage pipelined architecture. A scaling-down factor for the sampling capacitance and the input trans-conductance of amplifiers in each pipelined stage is decided to optimize conversion speed, power consumption, and thermal noise performance. A 3-D fully symmetric layout technique minimizes a capacitor mismatch in three multiplying D/A converters (MDACs) very much critical to the overall ADC linearity performance. The proposed ADC architecture is discussed in Section 2. Section 3 briefly describes circuit implementation and layout techniques. The measured results of the prototype ADC are summarized in Section 4. Finally, conclusion is given in Section 5.

2. PROPOSED ADC ARCHITECTURE

Commonly, in pipeline ADCs, the stage resolution (bit-per-stage) is decided considering linearity, maximum conversion rate, power consumption, and chip area. A single-bit-per-stage pipelined ADC architecture tends to have a higher maximum conversion speed than a multi-bit-per-stage architecture due to the decreased closed-loop gain and the reduced load capacitance of interstage amplifiers. However, deciding a single digital bit in each stage can result in increased pipelined stages, higher power consumption, larger chip area, and increased input-referred noise and device mismatch from the back-end pipelined stages. In contrast, the multi-bit-per-stage architecture deciding more digital bits in each stage requires less pipelined stages and lower power consumption with reduced chip area and decreased input-referred errors, while the increased closed-loop gain and the large load capacitance of interstage amplifiers can limit the maximum conversion speed of the ADCs [11].

Considering the above conflicting architectural issues, the proposed 14 b 150 MS/s CMOS ADC employs a four-stage pipelined architecture composed of an input SHA, three 4 b MDACs, three 4 b and one 5 b flash ADCs as illustrated in Figure 1. Two optimum scaling-down factors of pipelined stages, α_1 and α_2, are calculated and applied to the sampling capacitance and the input trans-conductance

Table I. Comparison of recently reported 14–15 b ADCs.

	[1]	[2]	[3]	[4]	[5]	[6]	[7]	[8]	[9]	[10]	This work
Resolution (bit)	14	14	14	14	14	14	14	14	15	15	14
Speed (MS/s)	50	70	75	80	100	100	100	125	40	40	150
Calibration	Y	N	N	Y	N	N	Y	N	Y	Y	N
Input range (V_{P-P})	2.0	2.0	2.0	2.0	2.0	—	1.6	2.0	2.1	2.3	1.0
SNDR (dB)	61	66	73	73	74	71	73	71	74	72	61
SFDR (dB)	84	81	88	70	90	86	91	70	93	90	70
DNL/INL (LSB)	0.5/1.0	0.6/1.8	0.6/2.0	0.4/0.6	—	0.8/2.1	0.9/1.3	0.2/0.5	0.3/4.0	0.3/1.5	0.8/2.8
Supply (V)	3.0	2.5	3.0	5.0	5.0	3.0	1.2	5.0	2.5	1.8	1.2
Power (mW)	350	235	340	1200	1250	230	250	1850	370	400	140
Area (mm^2)	16.0	3.3	7.8	—	28.5	7.28	1.0	70.0	13.7	20.0	2.0
FoM (pJ/conv.)	4.83	2.16	1.16	3.66	3.05	0.69	0.70	3.21	2.48	3.22	1.02
Process	0.18 um	0.13 um	0.35 um	0.35 um	0.8 um	0.18 um	90 nm	0.35 um	0.25 um	0.18 um	0.13 um
	CMOS	CMOS	CMOS	Bi-CMOS	Bi-CMOS	CMOS	CMOS	Bi-CMOS	CMOS	CMOS	CMOS

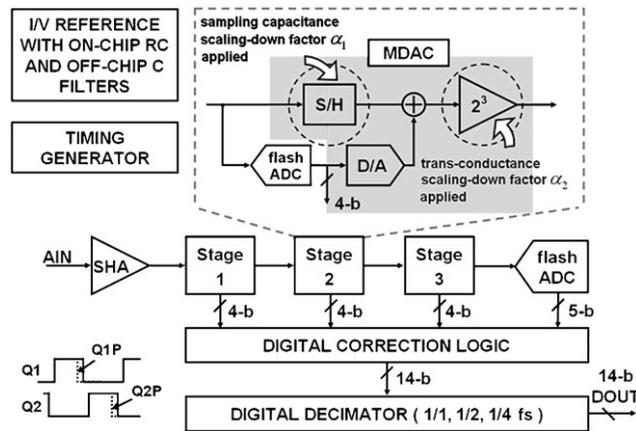**Figure 1.** Proposed 14b 150 MS/s 0.13 μm CMOS ADC.

of amplifiers in three MDACs, respectively. Current and voltage (*I/V*) references, digital circuits such as digital correction logic (DCL), decimator, and timing generator are integrated on-chip while two nonoverlapping timing clocks Q1 and Q2 are internally generated from a single external master clock. Nonlinear errors such as offsets and clock feed-through errors between pipelined stages are digitally corrected in the DCL by overlapping 3 b from 17 b raw codes to obtain 14 b final outputs. The on-chip decimator samples the 14 b outputs from the prototype ADC at a full, a half, or a quarter conversion rate to evaluate the ADC dynamic performance as accurately as possible by minimizing the glitch and transient noise coming from the evaluation board.

3. CIRCUIT IMPLEMENTATION AND LAYOUT TECHNIQUES
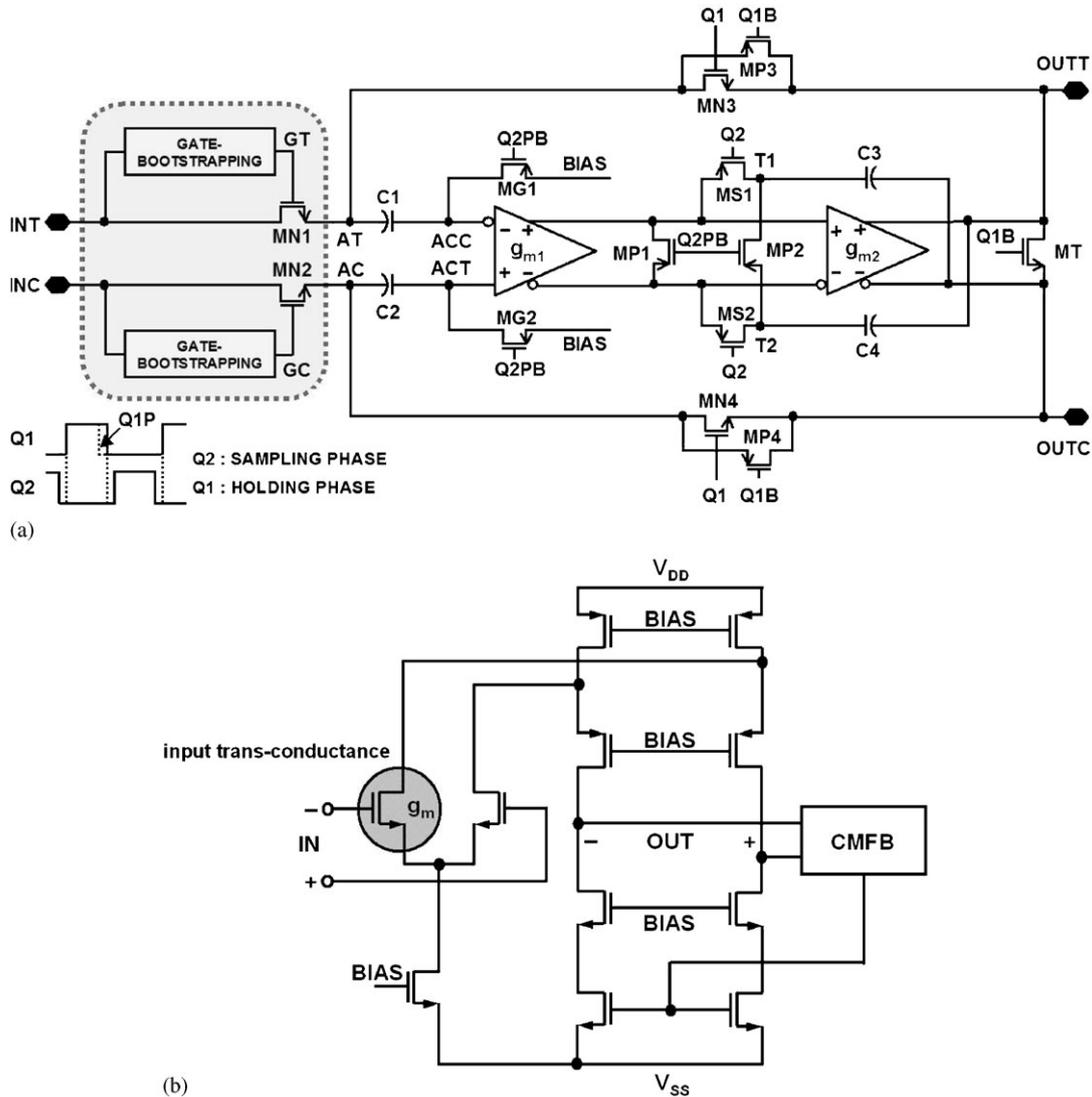
3.1. Wide-band low-noise input SHA

The wide-band low-noise input SHA based on a conventional two-capacitor flip-around circuit minimizes power consumption and chip area at 14 b and a sampling rate of 150 MS/s as illustrated in Figure 2(a) [12]. The SHA employs gate-bootstrapping input sampling switches as highlighted in Figure 2(a) to keep the gate-source voltage of sampling switches constant to minimize the nonlinear distortion of sampled inputs as well as to obtain an input sampling accuracy exceeding 14 b [13] In addition, a two-stage amplifier with the folded-cascode architecture meets the requirement of a high DC gain over 80 dB and the specific amplifier schematically employed in this work is illustrated in Figure 2(b). The phase margin of the amplifier is decided by observing the output signal settling behavior of the SHA and by optimizing the input trans-conductance ratios of the two-stage amplifier based on the loading conditions. When a phase margin is about 77° in this work, the output signal is reliably settled down within a required conversion time for 150 MS/s without any overshoot and undershoot. The sampling capacitance of the SHA is 8 pF

considering the required 14 b accuracy and kT/C noise at a $1.0 V_{p-p}$ full-scale input.

3.2. Pipelined stage scaling to optimize noise, conversion rate, and power consumption

Scaling-down techniques of the sampling capacitance and the trans-conductance of amplifiers in each succeeding stage have been widely employed in conventional pipelined ADCs. Such scaling-down techniques minimize the power consumption of ADCs without sacrificing the target sampling rate and the required noise performance [14, 15]. In a previously published paper, a scaling-down factor for back-end pipelined stages was decided by considering primarily one of many factors affecting speed, noise performance, and power dissipation such as the sampling capacitance and the trans-conductance of amplifiers [14]. In the other calculation, almost all of the factors above were considered only with the same scaling-down factor [15]. However, it is hard to obtain a performance-optimized scaling-down factor with those well-known approaches due to the complicated co-relation between various factors. In this work, two independent scaling-down factors, α_1 and α_2, respectively, for the sampling capacitance and the input trans-conductance of amplifiers are introduced and calculated to optimize the performance of noise, sampling speed, and power consumption of the proposed ADC.

Pipelined stages employed in this work are briefly described in Figure 3(a) where each stage includes a sampling capacitor and a two-stage amplifier. The definition of a feedback factor is summarized in Figure 3(b) and each stage has a feedback factor of around $\frac{1}{8}$. A scaling-down factor α_1 is applied to the sampling capacitor. The sampling capacitance in Stage1, Stage2, and Stage3 are indicated as C_S, $\alpha_1 C_S$, and $\alpha_1^2 C_S$, respectively. On the other hand, the parameters, g_{m1}, $\alpha_2 g_{m1}$, and $\alpha_2^2 g_{m1}$ represent the input trans-conductance of the first-stage amplifiers in Stage1, Stage2, and Stage3 with a scaling-down factor α_2, while

Figure 2. (a) Proposed wide-band low-noise input SHA and (b) folded-cascode amplifier used in the SHA and MDACs.

the input trans-conductance of the second-stage amplifiers in each stage are expressed as $g_{m2,1}$, $g_{m2,2}$, and $g_{m2,3}$, respectively. It is also noted that the sum of all the input trans-conductance of the first- and second-stage amplifiers of all three pipelined stages is represented as $g_{m,\text{tot}}$. This value of $g_{m,\text{tot}}$ is needed to find out scaling-down factors to optimize performance and power dissipation considering that the trans-conductance of amplifiers is proportional to the power consumption of amplifiers.

The primary two factors affecting the input-referred noise power of pipelined ADCs are the kT/C noise from sampling switches and the thermal noise occurred by the MOS transistors of amplifiers in each pipelined stage. The kT/C noise and the thermal noise from amplifiers are determined by the size of sampling capacitance and the input trans-conductance of amplifiers, respectively. As a result, the optimized scaling-down factors minimizing

power consumption while satisfying the requiring noise performance can be obtained by a proper calculation considering the variables described above.

First, a scaling-down factor α_1 for the sampling capacitance is determined by considering kT/C noise. The sum of the kT/C noise power referred to the ADC input from sampling switches in Stage1, Stage2, and Stage3 is derived in (1), where C_S is the sampling capacitance used in MDAC1 (Stage1) and $A_{n,\text{in}}$ indicates a gain from the input of the ADC to the input of the Stage n. The inversely proportional relationship between the scaling-down factor α_1 and $P_{NS,\text{total}}$ can be observed from (1) and a plot of $P_{NS,\text{total}}$ with the increment of the scaling-down factor α_1 is illustrated in Figure 4(a). Considering a minimum scaling-down factor to meet the required noise power for 14 b, less than $P_{NS,\text{max}}$ in Figure 4(a), is desired for the minimized chip area and power consumption, a scaling-down factor
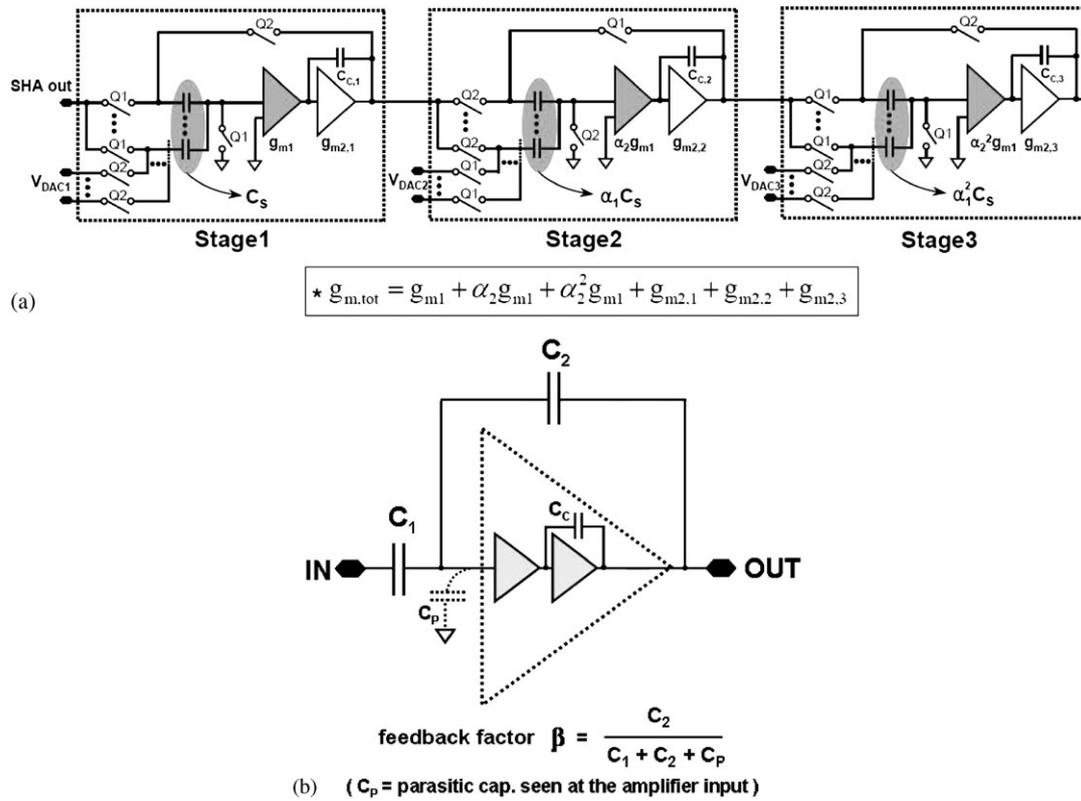
$$\star\ g_{m,tot} = g_{m1} + \alpha_2 g_{m1} + \alpha_2^2 g_{m1} + g_{m2.1} + g_{m2.2} + g_{m2.3}$$

(a)

$$\text{feedback factor}\quad \beta = \frac{C_2}{C_1 + C_2 + C_P}$$

(b)   (C_P = parasitic cap. seen at the amplifier input)

Figure 3. (a) Scaling-down factors α1 and α2 and (b) definition of a feedback factor β.
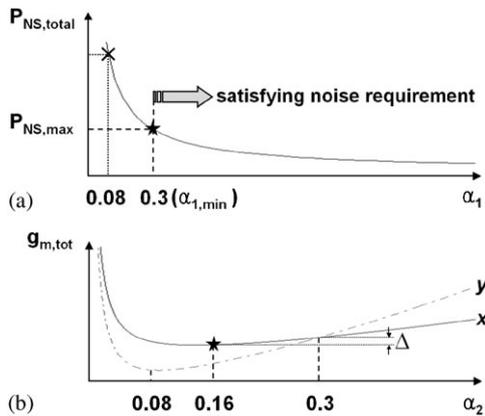

Figure 4. (a) Input-referred kT/C noise vs scaling-down factor α_1 of the sampling capacitance. (b) $g_{m,tot}$ vs scaling-down factor α_2 of the input trans-conductance of amplifiers.

α_1 is chosen to be 0.3 ($\alpha_{1,\min}$)

$$P_{NS,\text{total}} = \sum_{n=1}^{3} \left(\frac{kT}{\alpha_1^{n-1} C_S} \frac{1}{(A_{n,\text{in}})^2} \right) \tag{1}$$

Second, a scaling-down factor α_2 of the input trans-conductance of amplifiers can be obtained by taking (2) and (3) into calculation. Since the input trans-conductance of amplifiers is related to the stability as well as the noise power of amplifiers, the two equations representing the

input-referred noise power and the phase margin of the two-stage amplifier need to be considered. Equation (2) shows the input-referred noise power of the ADC due to the thermal noise of amplifiers in each stage, where $\omega_{-3\,\text{dB},n}$ and β_n are the required bandwidth and the feedback factor of Stage n while $A_{n,\text{out}}$ indicates a gain from the ADC input to the output of Stage n. Equation (2) is calculated from the power spectral density of the thermal noise referred to the differential input pair in a folded-cascode amplifier as shown in (4) and the output noise power of amplifiers as derived in (5) [16]. The phase margin of the two-stage amplifier is summarized in (3) where $C_{C,n}$ indicates the compensation capacitance used in Stage n and $C_{L,n}$ is the load capacitance seen at Stage n [17]. Especially, the load capacitance $C_{L,n}$ is the sum of the sampling capacitance of Stage $n+1$ ($\alpha_1^n C_S$) and the extra load capacitance observed at the output of the amplifier in Stage n ($C_{L,no}$).

$$P_{NA,\text{total}} = \sum_{n=1}^{3} \left(\frac{16kT \cdot \omega_{-3\,\text{dB},n}}{3\beta_n^2 \alpha_2^{n-1} g_{m1}} \frac{1}{(A_{n,\text{out}})^2} \right) \tag{2}$$

$$\phi_{PM,n} = 90^\circ - \tan^{-1}\left(\frac{\alpha_2^{n-1} g_{m1}}{C_{C,n}} \frac{C_{L,n}}{g_{m2,n}} \right) \quad \text{where}$$

$$C_{L,n} = \alpha_1^n C_S + C_{L,\text{no}} \tag{3}$$

$$S_V(f) = \frac{64kT}{3g_{m1}} \tag{4}$$

$$P_{NA} = \int_0^\infty S_V(f)|A_f(j2\pi f)|^2 \, \mathrm{d}f$$

$$= \int_0^\infty \frac{64kT}{3g_{m1}} \left| \frac{1/\beta}{1+(j2\pi f/\omega_{-3dB})} \right|^2$$

$$\mathrm{d}f = \frac{16kT \cdot \omega_{-3\mathrm{dB}}}{3\beta^2 g_{m1}} \tag{5}$$

Assuming that the maximally allowable noise power for a 14 b-level SNR is assigned to $P_{NA,\text{total}}$ in (2), the input trans-conductance of the first-stage amplifier in each stage (g_{m1}, $\alpha_2 g_{m1}$, $\alpha_2^2 g_{m1}$) with the increment of α_2 can be calculated. Once g_{m1}, $\alpha_2 g_{m1}$, and $\alpha_2^2 g_{m1}$ are decided, the input trans-conductance of the second-stage amplifier in each stage ($g_{m2,1}$, $g_{m2,2}$, $g_{m2,3}$) satisfying the phase margin over $60°$ is calculated by using (3) with the previously calculated scaling-down factor α_1. As a result, the input trans-conductance pairs calculated from Equations (2) and (3) simultaneously meet the noise performance and the stability of amplifiers in each stage. Considering that the summation of those input trans-conductance pairs, $g_{m,\text{tot}}$, is proportional to the overall ADC power consumption and also dependent on α_2, a power-optimized scaling-down factor can be found by searching the minimum value of $g_{m,\text{tot}}$ with increasing α_2. The calculated $g_{m,\text{tot}}$ with an increasing scaling-down factor α_2 from 0 to 1 is plotted as x in Figure 4(b). It is noted that all of the input trans-conductances (g_{m1}, $\alpha_2 g_{m1}$, $\alpha_2^2 g_{m1}$, $g_{m2,1}$, $g_{m2,2}$, and $g_{m2,3}$) deciding $g_{m,\text{tot}}$ automatically satisfy the noise, speed, and stability requirement of amplifiers with any α_2 from 0 to 1. Thus, the power minimized scaling-down factor α_2 becomes 0.16 as illustrated in the curve x of Figure 4(b) where the $g_{m,\text{tot}}$ shows the minimum value.

For comparison, the $g_{m,\text{tot}}$ calculated with a single scaling-down factor α ($=\alpha_1=\alpha_2$) for both of the sampling capacitors and the input trans-conductance of amplifiers is indicated in Figure 4(b) as y. As observed from the curve y, the scaling-down factor α ($=\alpha_2$) minimizing power consumption is 0.08. However, when applying this value simultaneously to the scaling factor α_1 of the sampling capacitance, the resulting $P_{NS,\text{total}}$ is higher than the required maximum noise power $P_{NS,\text{max}}$ as shown in Figure 4(a). To meet the overall noise requirement due to the kT/C noise, the scaling-down factor α_2 needs to be chosen as at least 0.3. However, choosing 0.3 for α_2 in the curve y results in a larger $g_{m,\text{tot}}$ than choosing 0.16 for α_2 in the curve x by Δ. This analysis shows that an improved power optimization can be obtained only by employing two separated scaling factors of α_1($=0.3$) and α_2($=0.16$) as discussed in this ADC design.

3.3. Highly linear 4 b MDACs based on signal-insensitive 3-D fully symmetric layout

Capacitor mismatch critically degrades the overall linearity of the pipeline stages [17, 18]. The capacitor mismatch is caused primarily by random errors and systematic errors. Process variations such as inaccurate etching and oxide thickness variations induce random errors, while systematic errors are coming from different parasitic capacitances between capacitors and adjacent signal lines. A variety of calibration techniques have been invented to overcome device mismatch problems for high-resolution exceeding 14 b. However, calibration techniques require additional circuit hardware blocks and timing cycles with the corresponding increased power consumption and chip area. High capacitor matching accuracy can be achieved simply by a proper signal-insensitive layout technique. The proposed signal-insensitive 3-D fully symmetric capacitor layout for high matching is shown in Figure 5 is based on the metal–insulator–metal (MIM) capacitor structure using seven metal lines in a 1P8M CMOS process. In Figure 5, all the symmetric unit capacitors are enclosed by all other metals except the metals for routing the top and bottom plates of capacitors. These unit capacitors isolated from all the neighboring signal lines minimize the capacitor mismatch physically and functionally. Capacitor mismatch can be further reduced by placing an extra metal layer connected to a fixed bias voltage under the bottom plate of each unit capacitor making the bottom parasitic capacitance of each unit capacitor similar. The extra metal layer cannot be located too close to the bottom plate, which increases the bottom plate parasitic capacitance further. The sum of all the unit capacitors in the MDAC1, MDAC2, and MDAC3 are 8, 2 and 0.8 pF, respectively, considering the required kT/C noise and the scaling-down factor α_1 described in Section 3.2.

4. PROTOTYPE ADC MEASUREMENTS

The proposed 14 b 150 MS/s ADC is fabricated in a 0.13 µm 1P8M CMOS process. The die photograph of the prototype ADC is shown in Figure 6, where the blocks encircled by bold and dashed lines represent on-chip PMOS and NMOS decoupling capacitors, respectively, for the suppression of the EMI problems and the random noise coupling from different functional circuit blocks.

The prototype ADC occupies an active die area of 2.0 mm^2 ($=1.52$ mm $\times 1.32$ mm) and dissipates 140 mW at 150 MS/s and 1.2 V. The measured differential nonlinearity (DNL) and integral nonlinearity (INL) are within 0.81LSB and 2.83LSB, respectively, as shown in Figure 7. A typical signal spectrum of the prototype ADC measured at 150 MS/s with a 1 MHz input and a 1.2 V supply voltage is plotted in Figure 8. Although several harmonic components of the fundamental input frequency can be observed, the harmonic effect on the overall linearity is relatively insignificant when compared with the thermal and quantization noise effects as analyzed below. Digital output data are captured at a quarter rate of the full conversion speed of 150 MS/s by the on-chip decimator to minimize digital coupling noise. The signal-to-noise-and-distortion
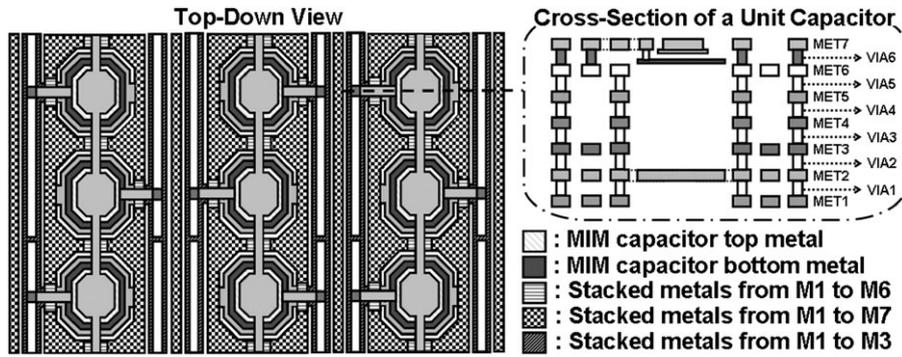
Figure 5. All signal isolated 3-D fully symmetric MDAC capacitors for high matching accuracy.

ratio (SNDR) and spurious-free dynamic range (SFDR) in Figure 9(a) are measured with different sampling frequencies up to 150 MS/s with a 1 MHz input. The SNDR and SFDR are maintained over 64 and 71 dB, respectively, up to 120 MS/s. With a maximum sampling frequency of 150 MS/s, the measured SNDR and SFDR are 61 and 70 dB, respectively.

The theoretically achievable maximum SNR$_{thermal}$ can be summarized in (6). Equation (6) is based on the sinusoidal input signal power with a peak-to-peak amplitude of V_{P-P} of (7), the 14 b-level quantization noise power of (8), and the input-referred thermal noise power coming from the sampling switches (kT/C noise) and the MOS transistors of amplifiers in the SHA and MDAC1 of (9). It is noted that only a half path of a differential pair is considered for simplicity.

$$SNR_{thermal} = 20\log\left(\frac{V_{rms}}{\sqrt{N_Q^2 + N_T^2}}\right) \quad (6)$$

$$\frac{1}{2}V_{rms} = \frac{0.5V_{P-P}}{2\sqrt{2}} \quad (7)$$

$$N_Q = \sqrt{\frac{1}{12}}\frac{0.5V_{P-P}}{2^{14}} \quad (8)$$

Figure 6. Die photograph of the prototype 14 b 150 MS/s ADC (1.52 mm × 1.32 mm).

and MDAC1. Those values are 8, 4.2 and 1.2 pF, respectively. Substituting these physical values for the above equations, the maximally acquired SNR$_{thermal}$ is 68 dB, which is comparable to a peak measured SNDR of 66 dB at a sampling rate of 40 MS/s as illustrated in Figure 9(a). Since any distortion is not included in the derived
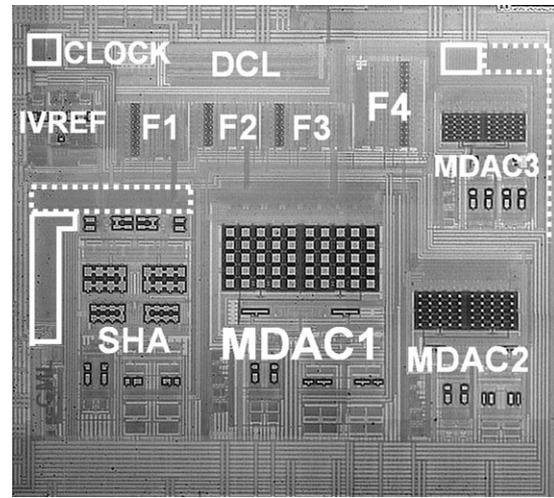
$$N_T = \sqrt{\frac{1}{2}(P_{NS} + P_{NA})}$$

$$= \sqrt{\frac{1}{2}\left\{\frac{4kT}{C_S} + \frac{16kT}{3}\left(\frac{\omega_{-3dB,SHA}}{\beta_{SHA}^2 \cdot g_{m1,SHA}}\frac{1}{A_{SHA}^2} + \frac{\omega_{-3dB,mdac1}}{\beta_{mdac1}^2 \cdot g_{m1,mdac1}}\frac{1}{A_{mdac1}^2}\right)\right\}}$$

$$= \sqrt{\frac{2kT}{C_S} + \frac{8kT}{3}\left(\frac{1}{C_{CS}} + \frac{9}{64C_{CM1}}\right)}, \quad (9)$$

$$\left(\omega_{-3dB,SHA} = \frac{g_{m1,SHA}}{C_{CS}} \cdot \beta_{SHA}, \omega_{-3dB,mdac1} = \frac{g_{m1,mdac1}}{C_{CM1}} \cdot \beta_{mdac1}, A_{SHA} = 1, A_{mdac1} = 8\right)$$

In the above Equations (6)–(9) [19], C_S is an input sampling capacitance of the SHA while C_{CS} and C_{CM1} are frequency-compensation capacitance employed in the SHA

equations, this result shows that the measured SNDR very much closely matches to the theoretically predicted calculation only based on quantization and thermal noise.
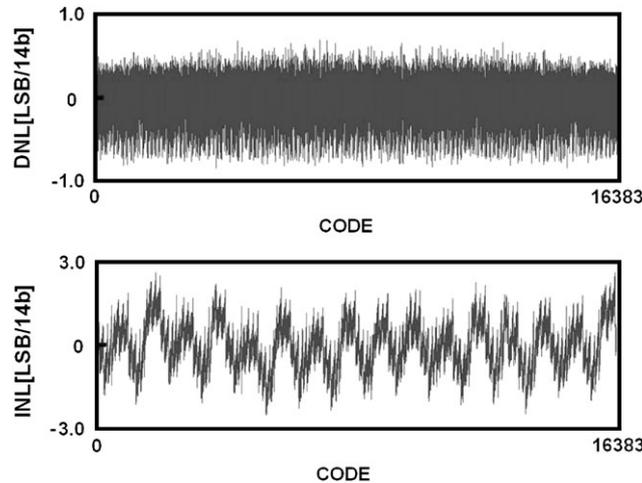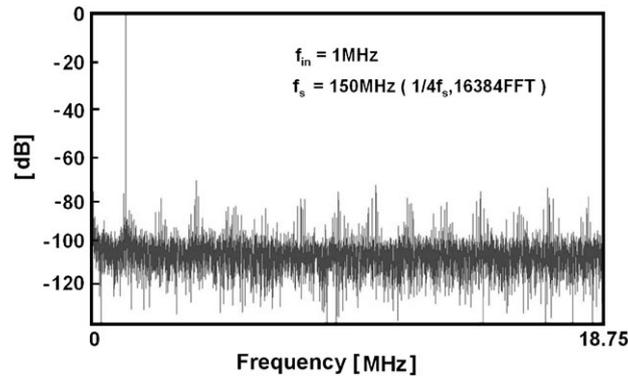
Figure 7. Measured DNL and INL.

Figure 8. Signal spectrum measured with a 1 MHz input signal at 150 MS/s.

Figure 9(b) shows the measured SNDR and SFDR with increasing input frequencies at a maximum sampling rate of 150 MS/s. With input frequencies increased to the Nyquist frequency, the SNDR and SFDR are maintained above 53 and 64 dB at 150 MS/s.

The theoretical SNR_{jitter} considering the input frequency and the clock jitter can be expressed in (10) where f_{in} and t_a denote the input frequency and the clock jitter, respectively [20]. When substituting the Nyquist rate input frequency of 75 MHz and the clock jitter of 4 ps caused by a clock generator used for the prototype ADC measurement to (10), the calculation result becomes approximately 54 dB.

$$SNR_{jitter} = 20 \log \left(\frac{1}{2\pi f_{in} t_a} \right) \qquad (10)$$

The theoretical value of 54 dB is quite close to the measured SNDR, which indicates that the measured SNDR at the Nyquist input frequency can be considerably restricted by the performance of a clock pulse generator in use. The clock jitter effect tends to be more critical to the maximum achievable dynamic performance when the resolution and sampling speed of the ADCs are increasing. Tables I and II summarize the performance

of the prototype ADC together with other comparable ADCs. Since the proposed design avoids various calibration techniques widely observed in the ADCs with a resolution exceeding 14 b, some performances such as SNDR, SFDR, DNL, and INL may not be the best of recently reported 14 b-level ADCs as shown in Table I. However, by eliminating complicated calibration circuits, the power consumption and chip area of the prototype ADC are considerably reduced even at a sampling rate of 150 MS/s with a $1 V_{pp}$-level input. The proposed ADC demonstrates a competitive figure of merits (FoM) of 1.02 pJ/conversion-step, defined as Power/($2^{ENOB} \times Fs$), compared with other works employing many inventive calibration techniques as summarized in Table I.

5. CONCLUSION

This work proposes a 14 b 150 MS/s 140 mW 2.0 mm^2 0.13 μm CMOS ADC for the SDR system as one of the next-generation communication technologies. A gate-bootstrapping technique and a properly g_m-ratioed two-stage amplifier are adopted in the front-end input SHA
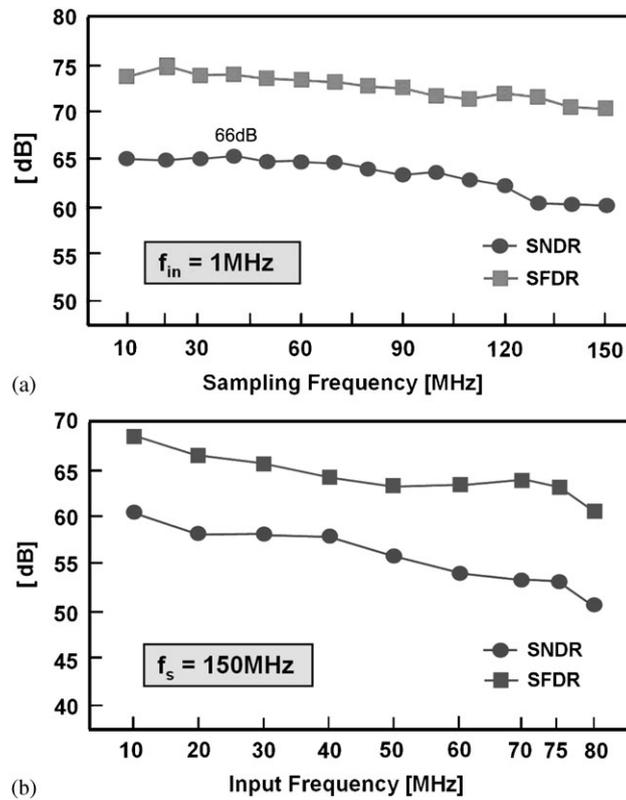
Figure 9. Measured SNDR and SFDR vs (a) fs and (b) fin.

Table II. Performance summary of the prototype ADC.

Resolution	14bits		
Conversion rate	40 MS/s (peak SNDR)	120 MS/s (typical)	150 MS/s (maximum)
Process		0.13 um 1P8M CMOS	
Input range		$1.0V_{P-P}$	
SNDR (at fin = 1 MHz)	66 dB	64 dB	61 dB
SFDR (at fin = 1 MHz)	74 dB	71 dB	70 dB
DNL		−0.81LSB/+0.59LSB	
INL		−2.66LSB/+2.83LSB	
ADC core power		140 mW at 1.2 V	
Active die area		2.0 mm^2 (= 1.52 mm × 1.32 mm)	

for high linearity and phase margin during high-speed operation. The proposed 14b ADC employs a four-stage pipelined architecture, while optimum scaling-down factors are separately applied to the sampling capacitance and the input trans-conductance of amplifiers in each stage simultaneously to optimize power consumption and noise performance at the target resolution and speed. A signal insensitive high-matching 3-D fully symmetric layout in three MDAC capacitor arrays minimizes capacitor mismatch by isolating critical unit capacitors from all neighboring signal lines without calibration. The prototype ADC implemented in a 0.13 μm 1P8M CMOS technology demonstrates a measured DNL and INL within 0.81LSB and 2.83LSB, respectively. The prototype ADC shows a maximum SNDR of 64 and 61 dB and a maximum SFDR of 71 and 70 dB at 120 and 150MS/s, respectively. The ADC occupies an active area of 2.0 mm^2 and consumes 140 mW at 150MS/s and a 1.2 V supply.

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